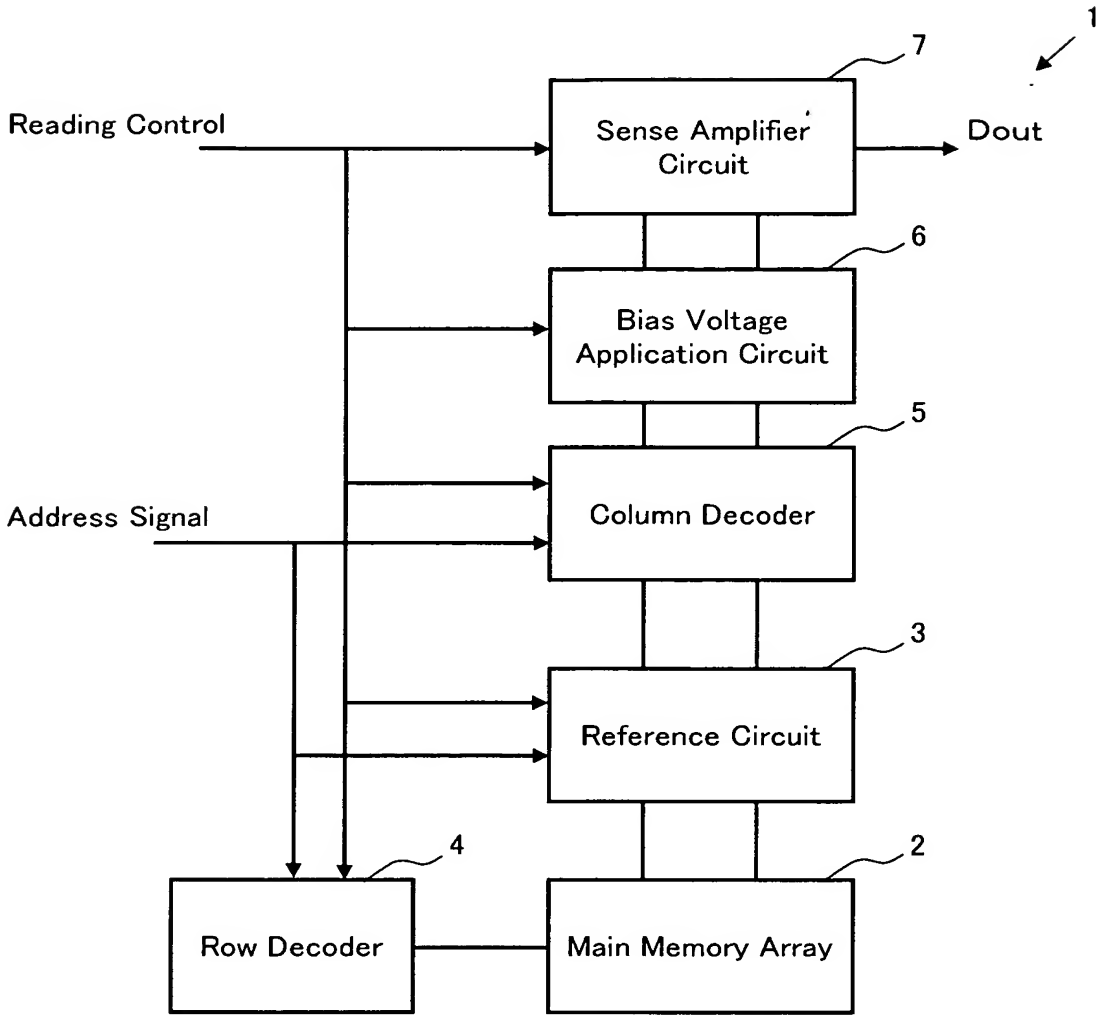
1
7
Reading Control
Sense Amplifier Circuit
Dout
6
Bias Voltage Application Circuit
5
Address Signal
Column Decoder
3
Reference Circuit
4
2
Row Decoder
Main Memory Array

Fig. 1

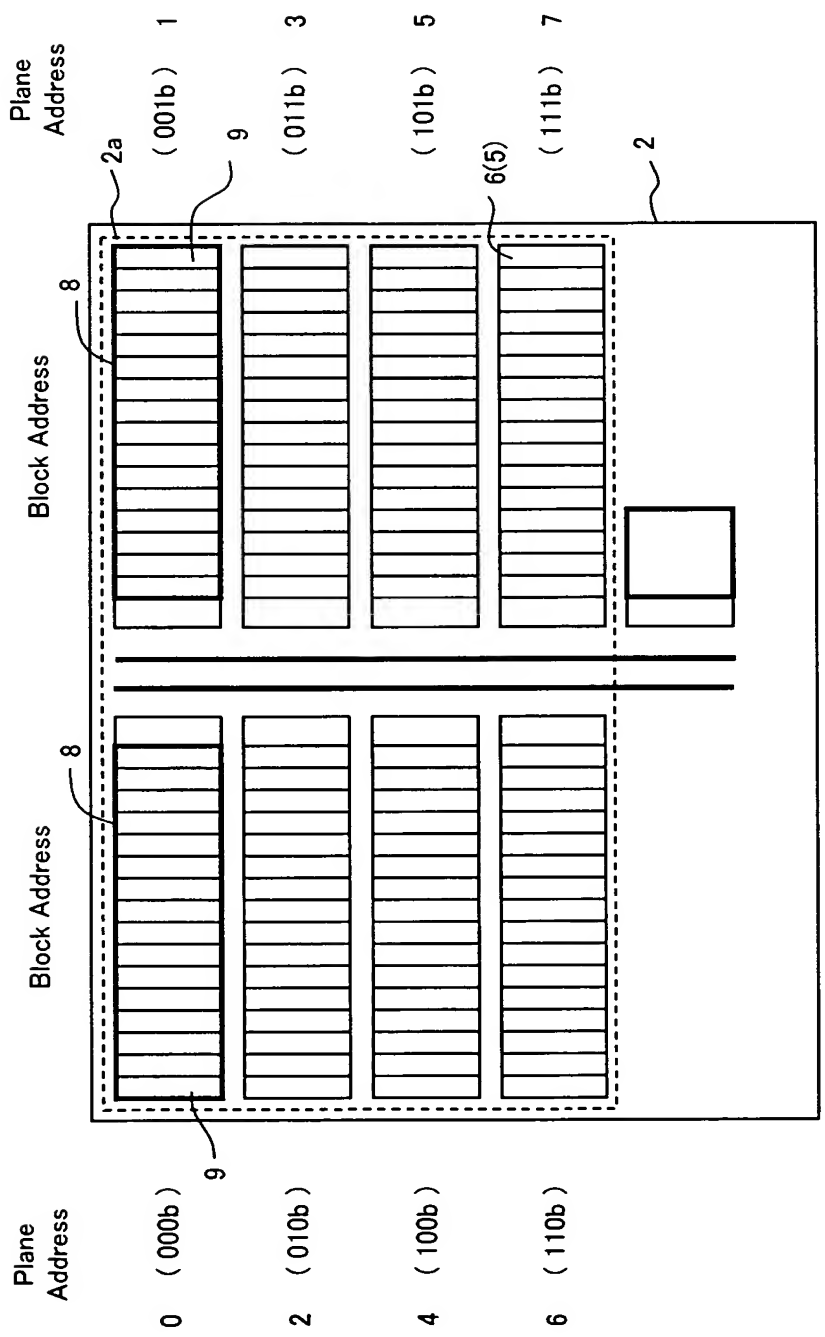
Plane Address
(001b) 1
(011b) 3
(101b) 5
(111b) 7
2a
9
6(5)
2
8
Block Address
8
Block Address
9
Plane Address
0 (000b)
2 (010b)
4 (100b)
6 (110b)

Fig. 2

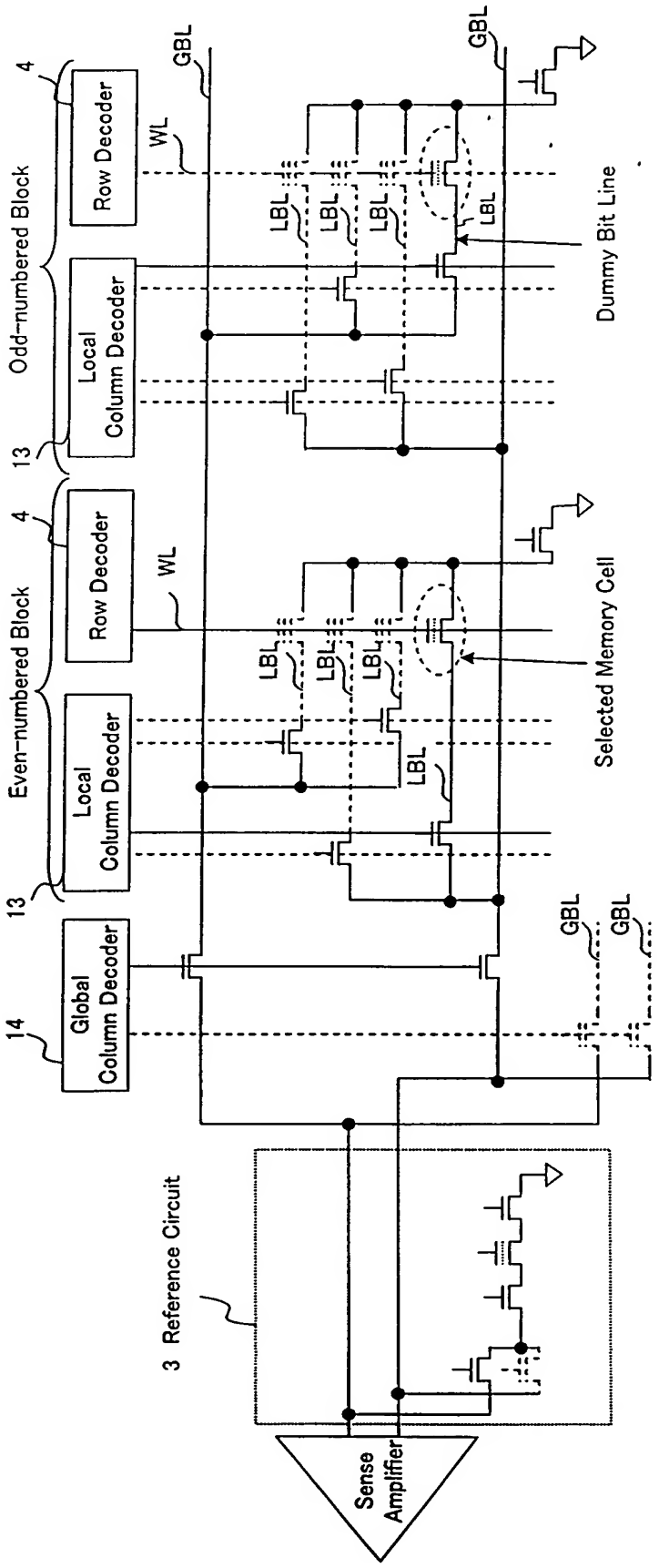
Row Decoder
Local Column Decoder
Odd-numbered Block
Even-numbered Block
Global Column Decoder
Reference Circuit
Sense Amplifier
WL
GBL
LBL
Dummy Bit Line
Selected Memory Cell
4
13
14
3

Fig. 3

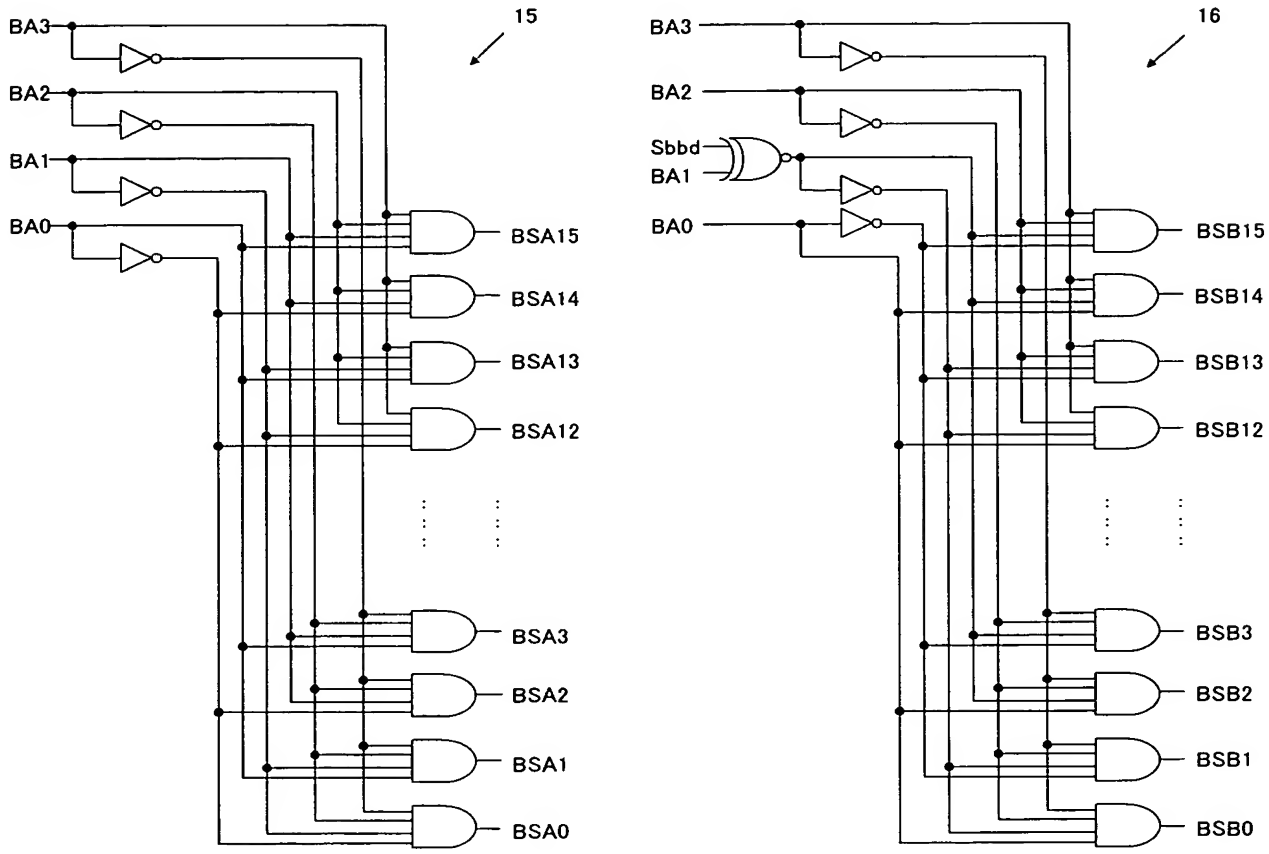
15
BA3
BA2
BA1
BA0
BSA15
BSA14
BSA13
BSA12
BSA3
BSA2
BSA1
BSA0
16
BA3
BA2
Sbbd
BA1
BA0
BSB15
BSB14
BSB13
BSB12
BSB3
BSB2
BSB1
BSB0

Fig. 4

BA				BSA	BSB	BSB
3	2	1	0		Sbbs=0	Sbbs=1
0	0	0	0	0	1	3
0	0	0	1	1	0	2
0	0	1	0	2	3	1
0	0	1	1	3	2	0
0	1	0	0	4	5	7
0	1	0	1	5	4	6
0	1	1	0	6	7	5
0	1	1	1	7	6	4
1	0	0	0	8	9	11
1	0	0	1	9	8	10
1	0	1	0	10	11	9
1	0	1	1	11	10	8
1	1	0	0	12	13	15
1	1	0	1	13	12	14
1	1	1	0	14	15	13
1	1	1	1	15	14	12

Fig. 5

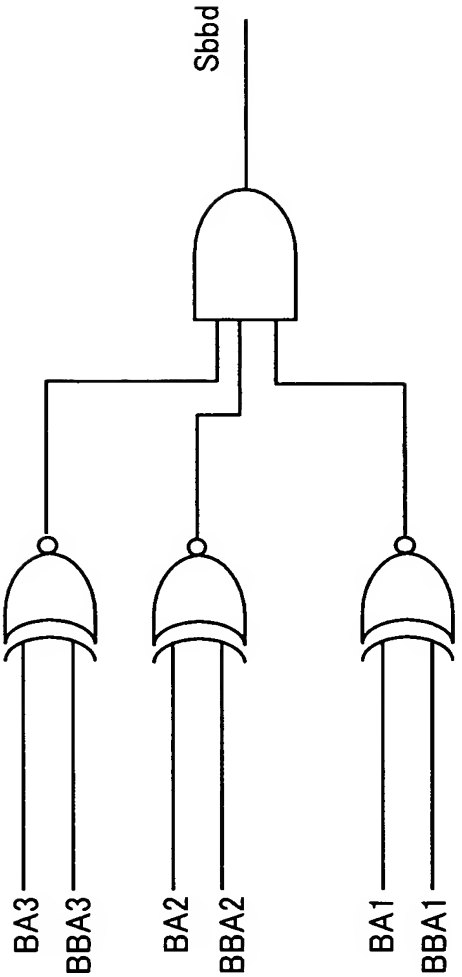

Fig. 6

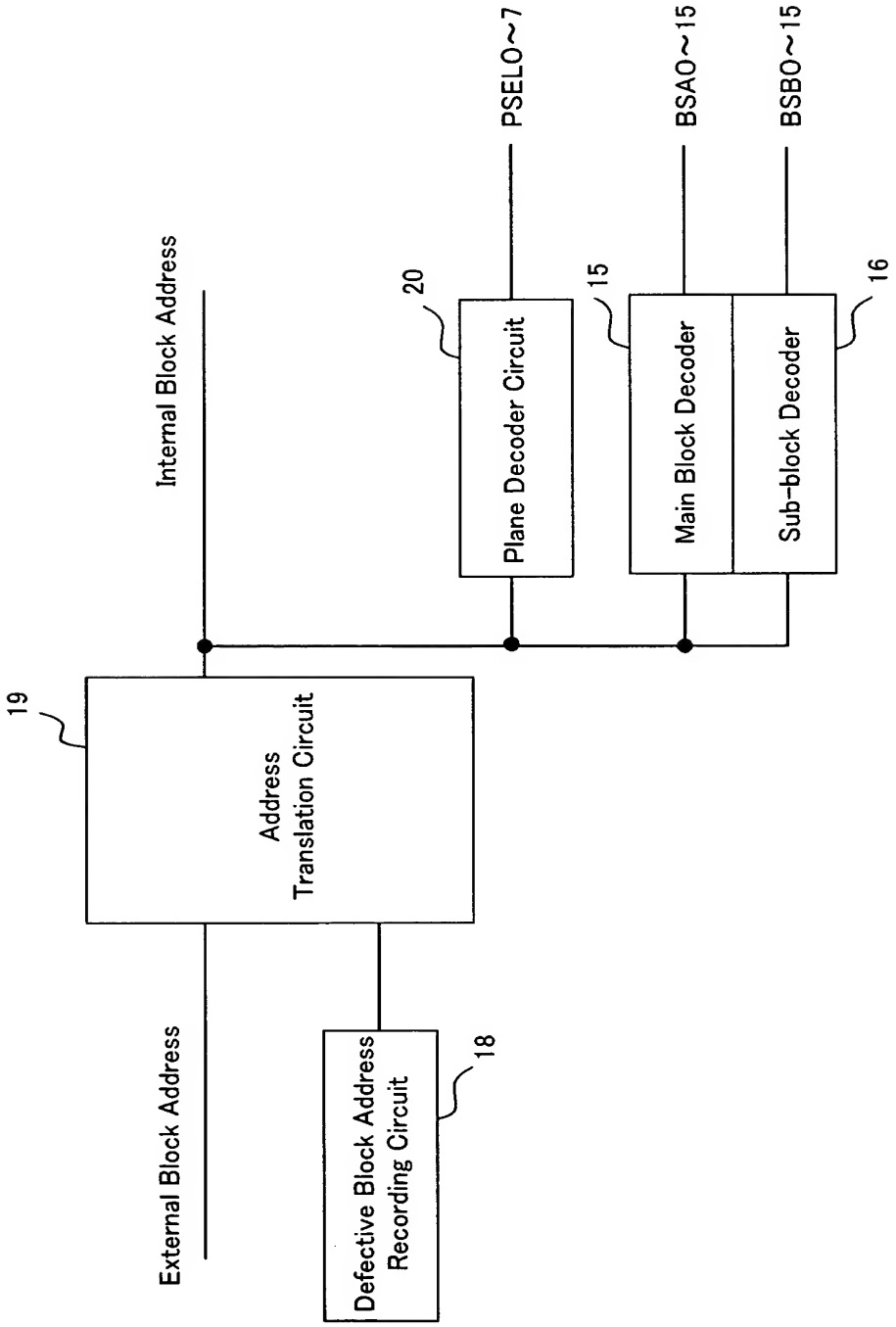
Internal Block Address
External Block Address
19
Address Translation Circuit
18
Defective Block Address Recording Circuit
20
Plane Decoder Circuit
PSEL0~7
15
Main Block Decoder
BSA0~15
16
Sub-block Decoder
BSB0~15

Fig. 7

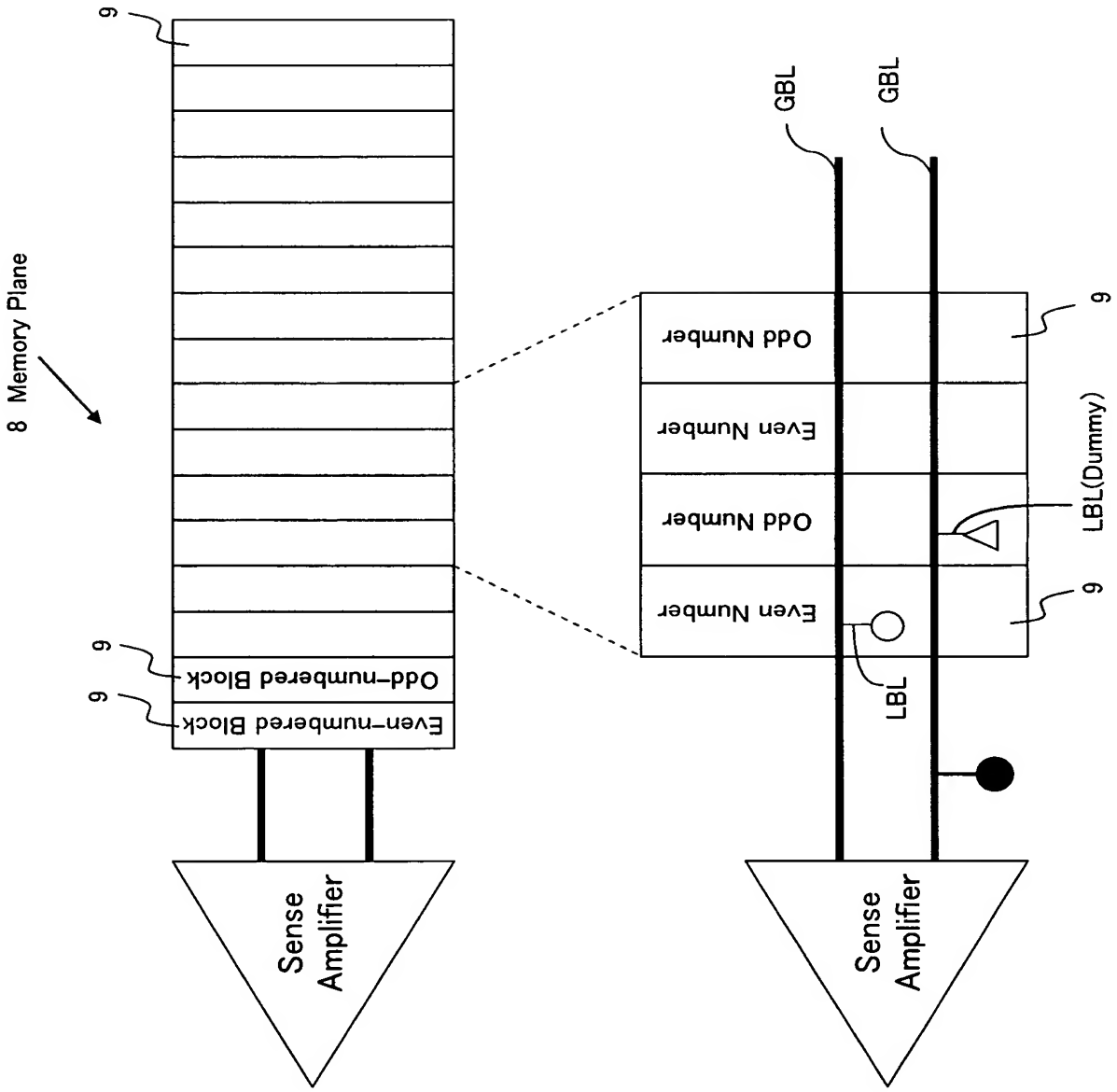
8 Memory Plane
9
Odd-numbered Block
Even-numbered Block
Sense Amplifier
GBL
GBL
Odd Number
Even Number
Odd Number
Even Number
LBL(Dummy)
LBL
Sense Amplifier

Fig. 8